



# Introduction to modeling and verification of digital systems

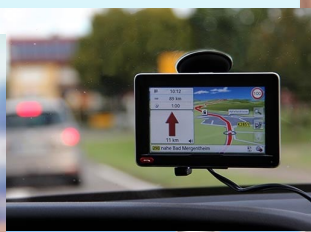
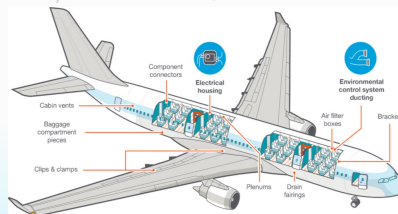
Laurence PIERRE  
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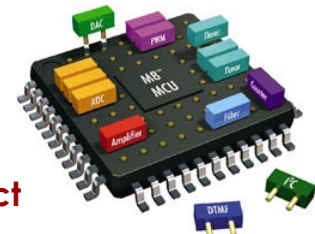
## Purpose

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### ■ Embedded system design



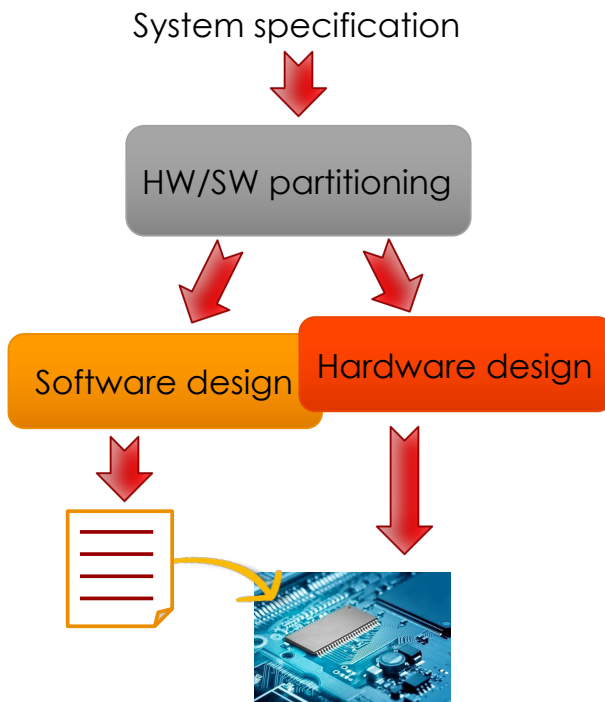
**Hardware** and **software** which **closely interact**



# Purpose

3

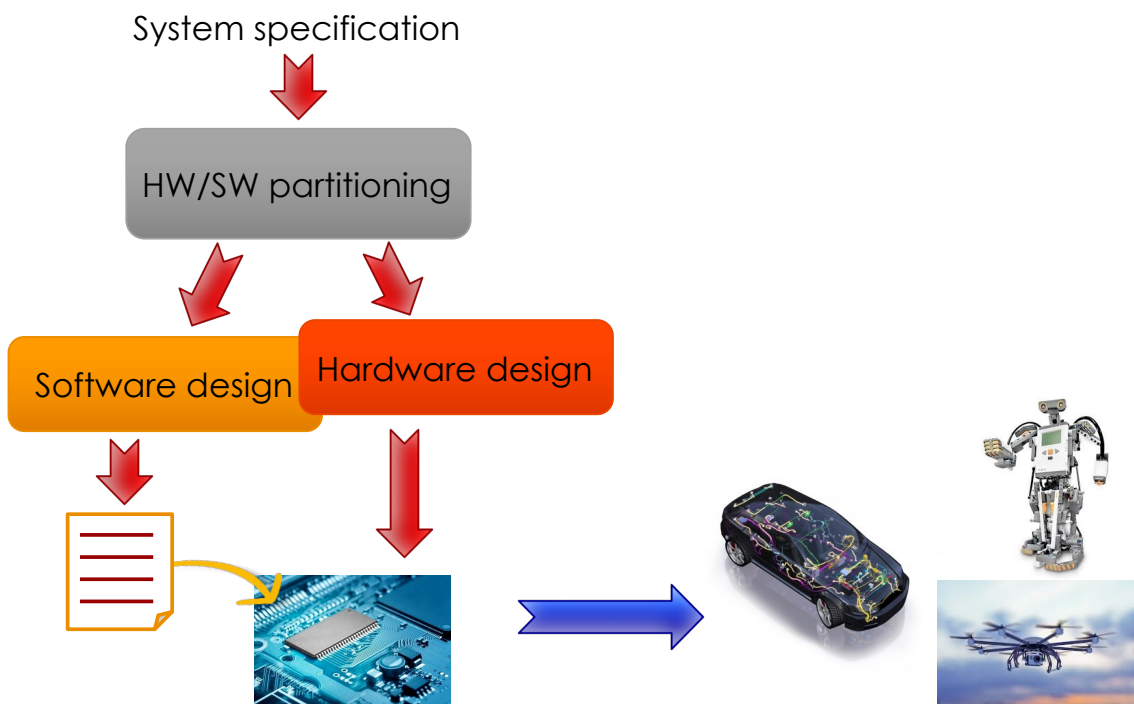
## ■ Embedded system design



# Purpose

4

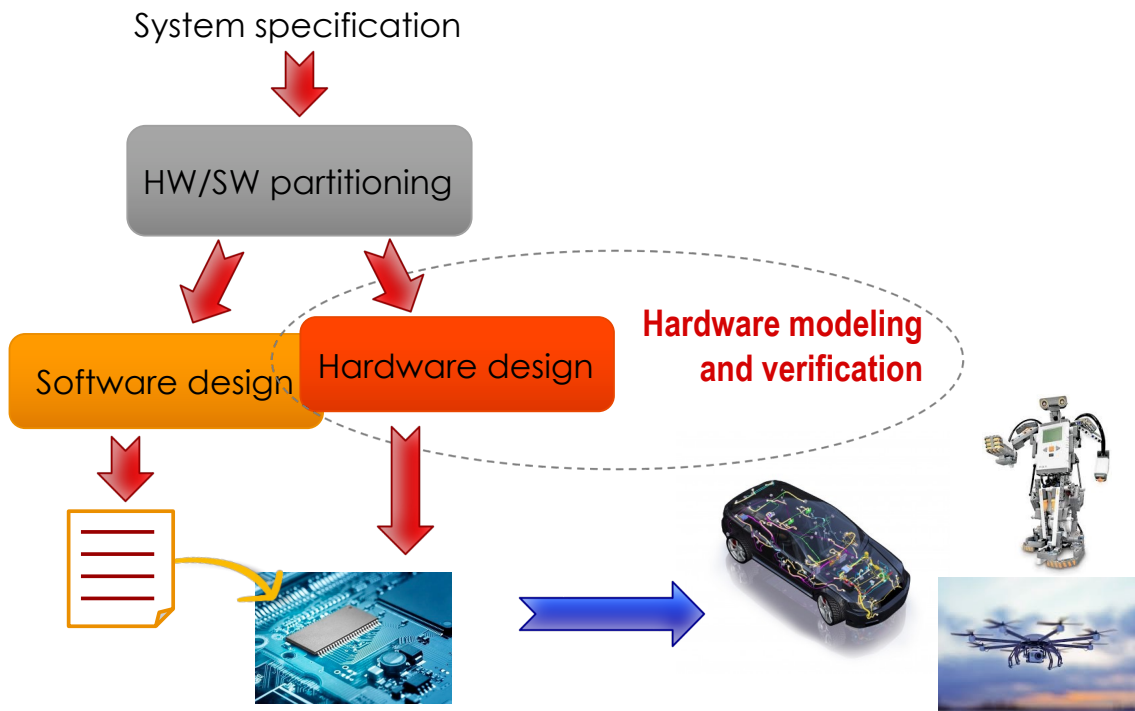
## ■ Embedded system design



# Purpose

5

## ■ Embedded system design

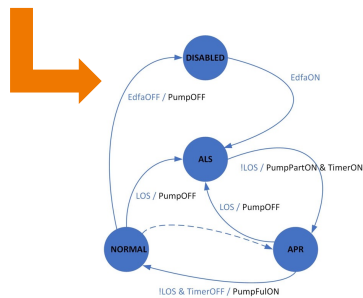


# Hardware design ?

6

In this course

Specification of the expected behaviour

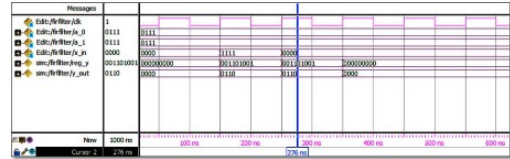
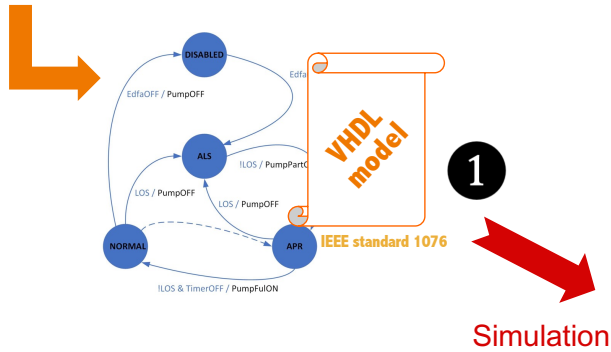


# Hardware design ?

In this course

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Specification of the expected behaviour

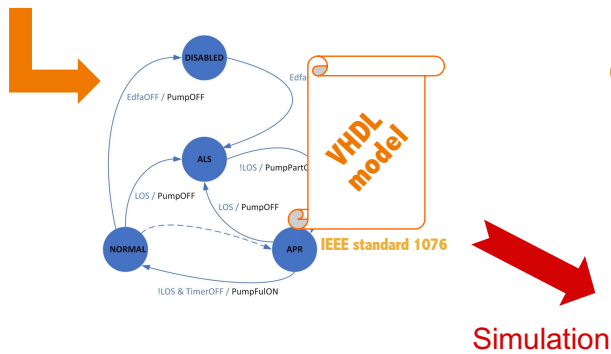


# Hardware design ?

In this course

8

Specification of the expected behaviour



Correctness properties  
(temporal assertions)



$$\begin{aligned} & (\neg b) U(a \wedge b) \\ & \square(a \rightarrow (\bigcirc \neg a \vee b)) \end{aligned}$$

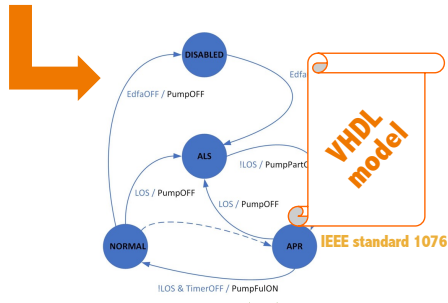


# Hardware design ?

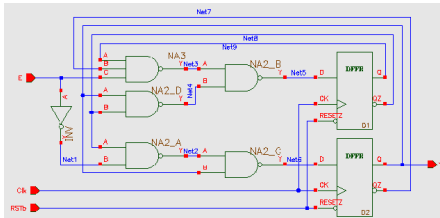
In this course

9

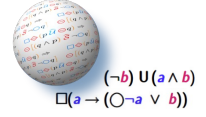
Specification of the expected behaviour



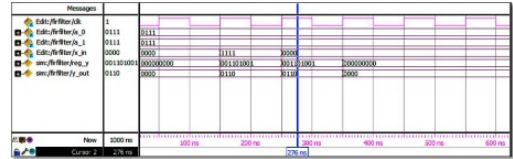
3 Logic synthesis (ASIC)



Correctness properties (temporal assertions)



Simulation

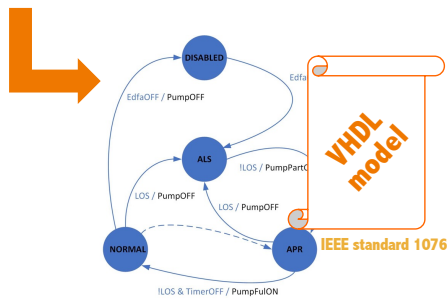


# Hardware design ?

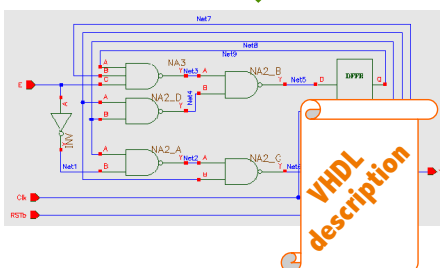
In this course

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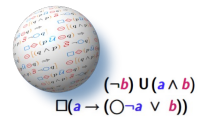
Specification of the expected behaviour



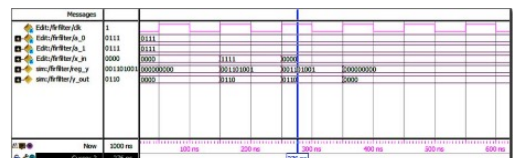
Logic synthesis (ASIC)



Correctness properties (temporal assertions)



Simulation



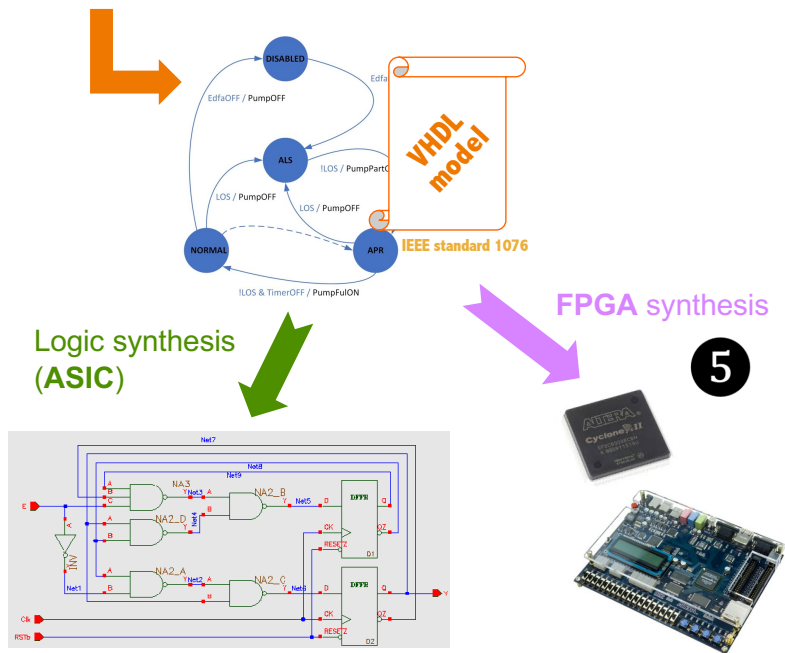
4

# Hardware design ?

In this course

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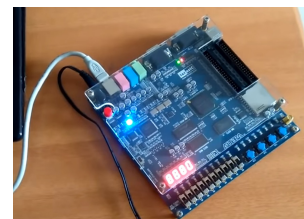
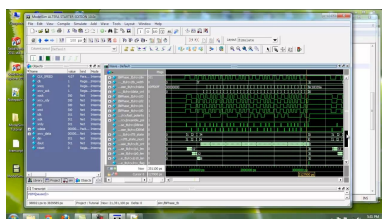
Specification of the expected behaviour



# Organization

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- **11 sessions**
  - 6 lecture+exercises sessions
  - 5 lab sessions
- **Prerequisite:** almost none
- **Assessment**
  - Complete project (5 lab sessions): from specification to FPGA, 50%



- Exam, 50%

- Lab sessions at **CIME Nanotech** (Centre interuniversitaire de microélectronique et nanotechnologies)
  - Use of **industrial software tools**

